



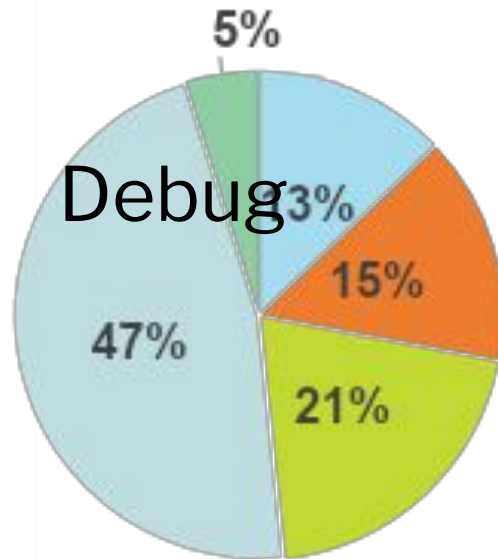
# Dragging Debug into a New Era

Front-End Design Engineering Track  
Monday, July 10th 1:30pm - 3:00pm PDT



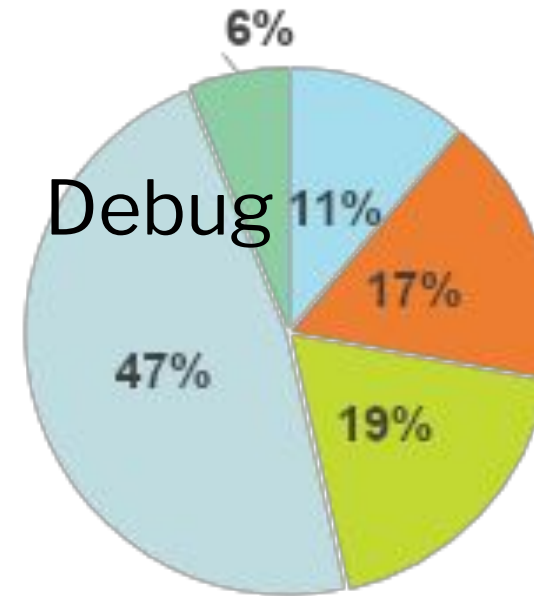
# Where verification engineers spend their time

## ASIC



This slide has not changed in Decades!

## FPGA



■ Test Planning ■ Testbench Development ■ Creating Test and Running Simulation ■ Debug ■ Other



# Accelerating Debug into a New Era

- Any slight change in the efficiency of this process gets magnified by scale
- Analytics and AI/ML have been chipping away
- Many other technologies to deploy







# Our Panel

- Andrew Ross—Director of Emulation Methodology & Infrastructure
  - *AMD*
- Eric Harris—Verification Lead
  - *Arm Ltd*
- Alan Pippin—Master Technologist
  - *Hewlett Packard Enterprise*
- Erik Berg—Principle SoC Verification Engineer
  - *Microsoft*

# Moderator

- Dave Rich—Verification Architect
  - *Siemens EDA*



# Questions for the Panel

1. Is debugging RTL much more complicated than debugging other programming languages? If true, why is it so hard?
2. Most people talk about debugging from simulator reports, what about static code analysis and formal-based debugging?
3. Debugging will still mainly be a human activity. Why are the current ML-based debugging tools so restrictive?
4. Many have realized the importance of data for debugging. With so much unstructured data, how do we apply ML here?
5. How important is data visualization for debugging?
6. Are we collecting too much data? How is that data being managed?
7. Where do you think the next breakthrough in applying ML for debugging will likely happen, why?
8. Where do you think ML will make breakthroughs, why?

